Sudarshan Sharma

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Research Interests

Secure and efficient implementation of Crypto Protocols, Hardware Security, Computer Architecture and Embedded Systems.

Education

- **Indian Institute of Technology (IIT), Kharagpur India** — **Current CGPA:8.66/10.00**
  B.Tech + M.Tech in Electronics and Electrical Communication Engineering — **2015-2020**
  with specialization in Microelectronics and VLSI Design
  Minor in Computer Science and Engineering
- **Delhi Public School, B.S City, Jharkhand, India** — **95.60%**
  Grade XII, All India Senior Secondary Central Examination (CBSE) — **2015**
- **Delhi Public School, Bhagalpur, Bihar,India** — **10.00/10.00**
  Grade X, Secondary School Certificate (CBSE) — **2013**

Publications

- **Sudarshan Sharma**, Dhruv Thapar, Nikhil Bhelave, and Mrigank Sharad "*Adaptive Multi-bit SRAM Topology Based Analog PUF*", in IEEE iSES 2019, Rourkela, India. *Accepted*[PDF]
- Gopabandhu Hota, **Sudarshan Sharma**, Aditya Rathore, Shailesh Joshi, and Het Shah "*An Integrated Visual Signalling, Localisation & Health Monitoring System for Soldier Assistance*", in IEEE ICECCT 2019, Coimbatore, India.[PDF]

White Papers/ Thesis

- "Primitives of Homomorphic Encryption: A Design Prespective" - *Master Thesis* [*Ongoing*] [Thesis]
- "Side Channel Attack on Block Cipher GIFT" - *Bachelor Thesis* [Slides]
- "KGPKubs Team Description Paper 2018: RoboCup Small Sized League" - *RoboCup, Montreal Canada 2018.*[PDF]
- "KGPKubs Team Description Paper 2017: RoboCup Small Sized League" - *RoboCup, Nagoya Japan 2017.*[PDF]

Internship

- **Flow to Identify Electron Migration (EM) Prone Structures** — **Qualcomm, Bangalore Design Center, India**
  Interim Engineering Intern, Memory Design Team — *May 2019-July 2019*
  Advisors: *Rahul Sahu, Senior Staff/Manager Engineer and Shiba Mohanty, Senior Lead Engineer*
  - Developed a tool to detect EM prone layouts using the **Calibre SVRF** rules and post processing using python in Samsung 5lpe.
  - Reviewed and designed the **read and write assist circuits** and compared the Voltage sense and Current sense amplifiers.
  - *Received a Pre-Placement offer to join the firm as a Memory Circuit Design Engineer.*
- **Acceleration of Neural Network Simulation with Binary Values for Logic Synthesis**[**PDF**] — **University of Tokyo**
  VDEC Intern, FUJITA Lab — *May 2018-July 2018*
  Advisor: *Prof. Masahiro Fujita, Director, VLSI Design and Education Center, University of Tokyo*
  - Worked on the development of a **CAD tool** for solving partial logic synthesis problem using discrete valued **DNN** architecture.
  - Modelled an approach based on And Inverted Graphs (**AIG's**) structure instead of existing Satisfiability (**SAT**) based solution.
  - Implemented existing discrete DNN training algorithm on **tensorflow** to train boolean functions from benchmarks
- **Car Electronics and Control Engineering** [**Certificate**] — **Pix Moving, China**
  Winter Intern, Guiyang — *Dec 2018*
  Advisor: *Sen Zeng, Mechanical Design & Automation Engineer*
  - Developed the **CAN system** comprising of the braking, steering and accelerator unit using 32 bit ARM Cortex M-3 microcontrollers.
  - Hacked the **BAIC EV car ultrasonic system** for parking assistance using the existing CAN Bus through statistical modelling.
  - *Received a Pre-Placement offer to join the firm as an Automation and Electronics Design Engineer.*

Research Experiences

- **Design of Homomorphic Encryption Primitives** [**PDF**] — **IIT Kharagpur**
  Master Thesis, SEAL Lab — *July 2019-Present*
  Advisors: *Prof. Debdeep Mukhopadhyay, Dept. of CSE and Prof. Indrajit Chakrabarti, Dept. of E&ECE*

- Designed fast and optimised **Gaussian Sampler** Architecture based on Knuth-Yao Algorithm using Xilinx FPGA fabrics.
- The project involves hardware and software co-design of Ring Learning with Error (RLWE) scheme including modular arithmetic modules like **Number Theoretic Transform** (NTT) and **bootstrapping techniques**.

- **Side Channel Attacks and Fault Analysis of Crypto Hardware** [PDF] **IIT Kharagpur**
  Bachelor Thesis, SEAL Lab *July 2018-Present*
  Advisor: *Prof. Debdeep Mukhopadhyay, Dept. of Computer Science and Engineering*
  - Working on Side Channel Attack on lightweight **block cipher** GIFT through correlation power analysis.
  - The project involves **RTL Design** of block cipher in Verilog, **Statistical modelling** of attacks based results and development of heuristic for best implementation.

- **Analog Physically Unclonable Functions**[PDF] **IIT Kharagpur**
  Undergraduate Researcher *June 2017-Present*
  Advisor: *Prof. Mrigank Sharad, Dept. of Electronics and Electrical Communication Engineering*
  - Designed a **robust, low power and area efficient** SRAM topology based multibit analog physically unclonable functions (PUFs).
  - The project involves circuit design, analysis and layout design on Virtuoso Cadence using Calibre DRC.Presently the chip is in layout phase and is expected to be submitted for fabrication using **scl180nm CMOS technology**.

- **Kharagpur Robosoccer Students' Group (KRSSG)**[Website] **IIT Kharagpur**
  ***Student Coordinator**, Electronics and Embedded Team* *Aug 2016-Present*
  Advisor: *Prof. Jayanta Mukhopadhyay, Dept. of Computer Science and Engineering*
  - Conceptualized and fabricated printed circuits boards based on AVR, ARM microcontrollers and FPGA architecture.
  - Designed and implemented a **proprietary BLDC motor controller** for the robots. Devised Verilog modules for close loop PID tuned Trapezoidal control of the BLDC motor and successfully optimised the communication system for least data loss.

- **Rehabilitation Robotics** **IIT Kharagpur**
  Algorithm Designer and Hardware Developer *Aug 2016-Present*
  Advisor: *Prof. Dilip Kumar Pratihar, Dept. of Mechanical Engineering*
  - Developed an **exoskeleton for the lower extremity** of the human body consisting of actuators and feedback sensors
  - Implemented a wireless network of RF modules, each node consisting of an IMU to record gait cycle data in the real time which send the data to RasPi for further processing, mimicked the actual gait cycle on the actuator of the exoskeleton using PID controller.

Training Experience

- **VLSI Summer School** **IIT Kharagpur**
  Student *May 2017-Jun 2017*
  Advisor: *Prof. Mrigank Sharad, Dept. of Electronics and Electrical Communication Engineering*
  - Designed a low noise amplifier for **bio-medical frontend** involving capacitive and active common-mode feedback using Cadence Virtuoso and LTSpice along with noise and stability analysis. Simulated RTL Design for hamming Distance using Xilinx ISE.

Projects

- **Design of Verilog Modules on Xilinx ISE**[PDF] [Code]
  VLSI Engineering Lab, Term Project *April 2018-May 2018*
  - Implemented 16 bit radix two and four **booth's multiplier** and various assignments on barrel shifters, fsm, scan chains and CORDIC.

- **Technologies for Soldier Support**[PDF]
  Inter-IIT Tech Meet 2018 *Dec 2017-Jan 2018*
  - Interfaced Flex sensors, IMU and trained CNN for the gesture identification module, Implemented an ad-hoc wireless localization framework using **Decawave** based radio modules and **LLS** algorithm, used Amitec SDRs to successfully achieve two way video transmission, health parameter monitoring modules included EEG, temperature and SpO2 probe.

- **ICCAD CAD Contest 2018**
  ICCAD 2018 *May-2018-Aug-2018*
  - Worked on Problem A: Smart EC: Program-Building for Name Mapping by **Cadence Design Systems, Inc** with team members from IITB and UTokyo. Secured Special Mention Award.

- **Linked Car**[PDF] [Code]
  Pet Project *Aug 2017-Jan 2018*
  - LinkedCar is a **V2X** platform which upgrades the cars of yesterday with the concepts of **Connected Autonomous Shared and Services and Electric (C.A.S.E.)** to harness the power of masses to enhance premium car experience.

- **Smart Steer**[PDF] [Code]
  Technology General Championship 2015-16 *Jan 2016-Mar 2016*
  - Structured the communication, localization and steering control, designed the main circuit of the autonomous wheelchair, integrated the bluetooth module with the mobile app.The team won the **GOLD** medal in the competition.

- **Person Following Turret**[Certificate]
  IEEE Certified Winter Workshop/Texas Instruments *Dec 2015*
  - Learned basics about **embedded electronics** and implemented it on various micro controllers- ATMEGA 16, Arduino.
  - Built a robot using three sonars and a servo motor capable of following the object using the triangulation technique.

Technical Skills

- **CAD Tools:** Xilinx (ISE and Vivado), Cadence (Virtuoso Analog Design Environment), Synopsys (Design & IC Compiler).
- **Microcontroller and Microprocessor:** AVR(Atmega), ARM Cortex Mx (STM), ARM Cortex A7 (Raspberry Pi).
- **Software/Scientific tool:** Git, LTSpice, Coocox CoIDE, Keil uVision, Atmel Studio, Eagle, Proteus.
- **Programming Languages:**C/C++, Python, MATLAB,

Proficient in Verilog Design, Algorithm to RTL Mapping, Xilinx FPGA Fabrics and Microcontroller based System Design.

Relevant Courses

- **VLSI Related Courses:** Digital Electronics Circuits*, Analog Electronics Circuits*, Semiconductor Device Modelling*, VLSI Engineering*, Architectural Design of IC's, VLSI for Telecommunications, VLSI CAD*, Analog VLSI, Digital VLSI, VLSI System Design and *VLSI Interconnects.*
- **Computer Science Related Courses:** Programming & Data Structures, Algorithms*, Hardware Security, Computer Architecture & Operating Systems and *Artificial Intelligence.*
- **Miscellaneous Courses:** Digital Signal Processing*, Micro controller & Embedded Systems*, Control System Engineering*, Analog Communication*, Digital Communication*, MIMO Communication and *Digital Signal Processing & Application*

*Courses with * have Theory as well as Laboratory hours. Courses in italics are currently ongoing*
[Link to Transcript]

Teaching Experiences

- **Digital Electronics Circuit Laboratory** **IIT Kharagpur**
  Teaching Assistant *May 2019-Nov 2019*
  Advisor: *Prof. Indrajit Chakrabarti, Dept. of Electronics and Electrical Communication Engineering*
  - Assisted third year undergraduate students with the experiments comprising of Combinatorial and Sequential Circuit design using TTL ICs on breadboards. Designed test materials and final evaluation.
- **IEEE Robotics Winter Workshop** **IIT Kharagpur**
  Project Head & Mentor *Dec-2016*
  - Mentored a group of 43 robotics enthusiasts from freshmen and sophomore year to build an Obstacle removing autonomous robot. Accomplished the Problem Statement in given time frame.

Position of Responsibility

- **Student Welfare Group** [**Certificate**] **IIT Kharagpur**
  Student Mentor *Jul 2017-Present*
  - Guiding a group of third year students of the institute to excel in academic as well as extra academic life under Student Mentorship Program under the Dean of Student's Affair, IIT Kharagpur.
- **Code-O-Soccer, KRSSG** [**Certificate**] **IIT Kharagpur**
  Student Co-ordinator *Feb 2015- Present*
  - Chaired Code-O-Soccer, a national coding event first of its kind, managed the in house prelims and workshop for the students. Responsible for the organising the event every year during Kshitij, IIT Kharagpur.

Extra-Curricular Achievements/Involvements

- Selected as **Captain** for Hardware Modelling Team, MS Hall for Technology General Championship 2019-20, IIT Kharagpur.
- Selected as an undergraduate representative for the university for Small Sized League **RoboCup Nagoya Japan 2017**.
- Represented IIT Kharagpur's **Gold** winning Contingent at Inter IIT Tech Meet, IIT Madras 2018.
- Secured, **First place** at the Xilinx Innovation Challenge during Kshitij 2018. Presented an Efficient Controller for Motors by harnessing parallelism and re-configurability of Xilinx FPGA and developed the same.[PDF]
- **Special Mention Prize** for Technical Innovative Approach at Hack.Bangalore 2018 a Digital Life.
- Secured 4th position in the **Finals** of event Anadigx (Analog and Digital Circuit Design Competition) during Kshitij 2017.
- Won the **Best Freshers Award** in a semi-autonomous event Warehouse during Kshitij 2016, IIT KGP.
- Secured **First Position** in the Robosapiens Hackathon held after the overnight Workshop during NSSC 2015, IIT KGP.
- Completed two years as **National Cadet Corps'(NCC)** Cadet, under Ministry of Defence,Government of India.

[Certificates]